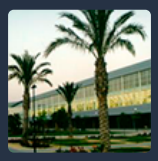

COMPUTER ARCHITECTURE

Universitat d'Alacant
Universidad de Alicante

34020 - COMPUTER ARCHITECTURE (2024-25)

General

Code: 34020
Lecturer responsible:
FUSTER GUILLO, ANDRES

Credits ECTS:	**6,00**
Theoretical credits:	1,20
Practical credits:	1,20
Distance-base hours:	3,60

Departments involved

- **Dept:** INFORMATION TECHNOLOGY AND COMPUTING
  Area: COMPUTER ARCHITECTURE
  Theoretical credits: 1,2
  Practical credits: 1,2
  This Dept. is responsible for the course.
  This Dept. is responsible for the final mark record.

Study programmes where this course is taught

- DEGREE IN COMPUTER ENGINEERING
  Course type: COMPULSORY (Year: 2)
- DOUBLE DEGREE IN COMPUTER ENGINEERING AND BUSINESS ADMINISTRATION
  Course type: COMPULSORY (Year: 3)

Competencies and objectives

Course context for academic year 2024-25

The Computer Architecture course forms part of the knowledge pertaining to the branch known as Architecture and Technology of Computers, branch among other things explains the operation of computers as computing machines.

This course is one of the key subjects in relation to the study of computer architectures and together with the courses of Computer Fundamentals and Computer Structure, complete aspects of theory, abstraction and design of the area.

Moreover, the course acts as a bridge introducing advanced architectures, whose contents will be consolidated in the third year course of Computer Engineering and other optional courses of the Computer Engineering route.

Its location and characterization as mandatory in the syllabus make it a course that explores various concepts introduced in Computer Structure, but considering that, while in the latter the computer is studied from the point of view of their functional units, in Computer Architecture the study is approached from a higher level, from an engineering perspective and considering issues related to the design, evaluation and strategies to increase performance while it serves as basis for the accomplishment of these objectives in the course of Computer Engineering.

The previous courses (Computer Fundamentals and Computer Structure) that students had to attend, expect that they reach the course with a reasonable knowledge base about architectures that, in any case, is necessary to analyse, consolidate, formalize and illustrate with specific implementations and designs, approaching that from a broader perspective, introducing, at the same time, new performance enhancing techniques.

Course content (verified by ANECA in official undergraduate and Master's degrees) for academic year {0}

Specific Competences (CE)

- **CE1 :** Capacitat per a dissenyar, desenvolupar, seleccionar i avaluar aplicacions i sistemes informàtics, assegurant la seua fiabilitat, seguretat i qualitat, d'acord amb principis ètics i amb la legislació i normativa vigent.
- **CE14 :** Coneixement i aplicació dels principis fonamentals i tècniques bàsiques de la programació paral·lela, concurrent, distribuïda i de temps real.
- **CE8 :** Capacitat per a analitzar, dissenyar, construir i mantenir aplicacions de forma robusta, segura i eficient, triant el paradigma i els llenguatges de programació més adequats.

Exclusive skill taught in this course

No data

Learning outcomes (Training objectives)

No data

Specific objectives stated by the academic staff for academic year 2024-25

The general objective of this course aims that the students know and strengthen key aspects of analysis, design and implementation of classic sequential architectures, the immediate improvements within this classic paradigm, and the existence of alternative architectures. As a basic working method, a set of tools and settings are established that allow students to study and analyse in greater depth and rigor different architectural options, combining the abstract and generic aspects with the study of specific implementations.

The specific objectives are specified in the following:

Cognitive objectives

- Define the concept of architecture and incorporate parameters to evaluate and analyze the performance
- Explain the impact of the ISA on the architecture and performance, understanding the design principles of the ISA
- Identify the pipelining as a basic technique for increasing CPU performance as well as design, planning and control of pipeline units
- Understanding the evolution of the architectures and the differences between CISC and RISC approaches
- Explain techniques for improving the performance of memory and input/output system
- Recognize the limitations of classical architectures and the importance of parallelism
- Know and use the usual terminology and the language of the subject and employ it correctly both orally and in writing

Skills

- Develop design skills of Instruction Sets
- Know how to design a pipelined datapath
- Understand the potential of a hierarchical memory system
- Be able to write benchmarks to evaluate specific aspects of computers
- Be able to use standard benchmarks to perform evaluation studies, and interpret the corresponding result reports

Attidunal

- Appreciate the importance of optimization of various components of the computer architecture to improve performance
- Develop critical thinking when evaluating the performance of a computer system according to objective criteria
- Ability to integrate into working groups involved in analysis and design tasks
- Capacity to make efforts in searching solutions and autonomous learning

Content and bibliography

Content for academic year 2024-25

Theoretical contents

- Unit 1. Introduction
  - 1.1 Computer architecture. Concepts and definitions
  - 1.2 Multileve architecture
- Unit 2. Performance evaluation
  - 2.1. Performance. Concepts and definitions
  - 2.2. Performance evaluation
- Unit 3. Instruction Set design
  - 3.1 Taxonomy of architectures at machine language level
  - 3.2 Memory addressing
  - 3.3 Instruction set
  - 3.4 Principles of design RISC computers
  - 3.5 Very large instruction word set
  - 3.6 Examples of IS
- Unit 4. Pipelining.
  - 4.1 Introduction
  - 4.2 Instruction pipelining
  - 4.3 Arithmetic pipelines
  - 4.4 Optimization of pipelined units
  - 4.5 Superscalars
- Unit 5. Memory system performance
  - 5.1 Memory hierarchy
  - 5.2 Cache memory
  - 5.3 Improving performance of main memory
  - 5.4 Virtual memory
- Unit 6. I/O system performance
  - 6.1 Measuring performance of I/O system
  - 6.2 Buses
  - 6.3 I/O devices

Practical contents

- Performance evaluation project
  - Background
  - Development of a performance evaluation program and performance evaluation of conventional PC architectures
  - Performance evaluation of GPGPU architectures

Related links

No data

Bibliography

Arquitectura de computadores	
Author(s):	Ortega Lopera, Julio ; Anguita López, Mancia
Issue:	Madrid : Thomson , 2005;
ISBN:	84-9732-274-6
Category:	Sin especificar

Organización y arquitectura de computadores	
Author(s):	Stallings, William
Issue:	Madrid : Pearson Prentice Hall, 2005;
ISBN:	978-84-8966-082-3
Category:	Sin especificar

Computer architecture : a quantitative approach	
Author(s):	Hennessy, John L.
Issue:	Cambridge Estados Unidos : Morgan Kaufmann , 2019;
ISBN:	978-0-12-811905-1
Category:	Básico

Assessment

Assessment procedures and criteria 2024-25

The course grade consists of 2 blocks. Block 1 (B1) is formed by the "Practice and practical reports" activity. Block 2 (B2) consists of activities "Control Theory" and "Problems of theory." The score of all activities is a numeric value between 0 and 10.

B1 = NP
B2 = 0.3*NT + 0.7*NPT

The final grade (NF) will be the result of the sum of scores on the various tests of established assessment, considering the proportion assigned to each. In addition, a minimum score of 4 in block B1 and B2 are required to pass the course. If a student does not overcome any of the minima in these two blocks, he/she cannot pass the course, being its grade the minimum value between the mark obtained and the value 4.5.

NF = 0.5*(B1+B2) iff B1 >= 4 and B2 >= 4

Otherwise, NF=min (0.5*(B1+B2), 4.5)

Optionally, individual theoretical or practical work to mark a maximum of 1 point. This work will be assessed if and only if it meets the minimum required in the blocks.

If the student has not been rated in all blocks, will be graded as "No presentiality". Otherwise, the grade will be proceed with the summation of all the marks accordingly.

The delay in the delivery of the documents of each practice will mean a reduction of the final grade for that practical assignment: A one-week delay will mean a reduction of 40% of the grade. With a longer delay practice does not qualify.

Description	Criteria	Type	Weighting system
Theoretical assessment	Two control theory tests (multiple choice questions / short questions / problems short) will be held for units 1, 2 (Test 1), 3 and 4 (Test 2). The note of controls (NT) is obtained as a weighted average of each control. This test can be retake in the second evaluation period by a final control of all theory units.	ACTIVITIES OF EVALUATION DURING THE SEMESTER	15
Practicals assessment	The Practical mark (PN) is obtained by continuous assessment of the contents of each practice and presenting a report at the end of it. Individual checks (multiple choice questions/short questions/short exercises) on the statements of practice will also be carried out. The final practical mark is the weighted average of the marks for each. This mark can be retake in the second evaluation period by a practical examination in the laboratory.	ACTIVITIES OF EVALUATION DURING THE SEMESTER	50
Problems assessment	A final exam will be performed to assess theoretical problems (NPT). This part can be retake in the second evaluation period.	FINAL TEST	35

Official exam dates for academic year 2024-25

Exam session	Date	Time	Group - Classroom(s) allocated	Comments
(C3) Periodo ordinario para asignaturas de segundo semestre y anuales	13/06/2025			Teoría
(C4) Pruebas extraordinarias para asignaturas de grado y máster	03/07/2025			Prácticas
	03/07/2025			Controles de teoría
	11/07/2025			Teoría

Academic staff

FUSTER GUILLO, ANDRES
Lecturer responsible

THEORY CLASS: Groups: 1 , 3 , 4 , 40
COMPUTER PRACTICALS: Groups: 01 , 03 , 04 , 05 , 06 , 02 , 401

AZORIN LOPEZ, JORGE

THEORY CLASS: Groups: 3

BARON BAUTISTA, MARIA CORPUS

THEORY CLASS: Groups: 40

COLOM LOPEZ, JOSE FRANCISCO

COMPUTER PRACTICALS: Groups: 01 , 05

CORTES PLANA, JOSE JUAN

THEORY CLASS: Groups: 4
COMPUTER PRACTICALS: Groups: 04

JIMENO MORENILLA, ANTONIO MANUEL

COMPUTER PRACTICALS: Groups: 02 , 401

ORTEGA CANDEL, JOSE MANUEL

COMPUTER PRACTICALS: Groups: 06

PERTEGAL FELICES, MARIA LUISA

COMPUTER PRACTICALS: Groups: 01

Groups

THEORY CLASS

Group	Semester	Morning or afternoon session	Language	No. of enrolled students	
Gr. 1 (THEORY CLASS) : 1	2S	Morning	Spanish	147	▪ Allowed DEGREE IN COMPUTER ENGINEERING
Gr. 2 (THEORY CLASS) : 2	2S	Morning	Spanish	0	
Gr. 3 (THEORY CLASS) : 2 (ARA)	2S	Morning	English	24	▪ Allowed DEGREE IN COMPUTER ENGINEERING
Gr. 4 (THEORY CLASS) : 3 VAL	2S	Afternoon	Valencian	21	▪ Allowed DEGREE IN COMPUTER ENGINEERING
Gr. 40 (THEORY CLASS) : 40 I2ADE	2S	Morning	Spanish	40	▪ Allowed VISITING STUDENT NO EEES ▪ Allowed VISITING STUDENT EEES ▪ Allowed INTERNATIONAL MOBILITY PROGRAMME ▪ Allowed DOUBLE DEGREE IN COMPUTER ENGINEERING AND BUSINESS ADMINISTRATION

COMPUTER PRACTICALS

Group	Semester	Morning or afternoon session	Language	No. of enrolled students	
Gr. 01 (COMPUTER PRACTICALS) : 1	2S	Morning	Spanish	39	▪ Allowed DEGREE IN COMPUTER ENGINEERING
Gr. 02 (COMPUTER PRACTICALS) : 2	2S	Morning	Spanish	40	▪ Allowed DEGREE IN COMPUTER ENGINEERING
Gr. 03 (COMPUTER PRACTICALS) : 3 (ARA)	2S	Morning	English	24	▪ Allowed DEGREE IN COMPUTER ENGINEERING
Gr. 04 (COMPUTER PRACTICALS) : 4 VAL	2S	Afternoon	Valencian	21	▪ Allowed DEGREE IN COMPUTER ENGINEERING
Gr. 05 (COMPUTER PRACTICALS) : 5	2S	Afternoon	Spanish	33	▪ Allowed DEGREE IN COMPUTER ENGINEERING
Gr. 06 (COMPUTER PRACTICALS) : 6	2S	Afternoon	Spanish	35	▪ Allowed DEGREE IN COMPUTER ENGINEERING
Gr. 07 (COMPUTER PRACTICALS) : 7	2S	Morning	Spanish	0	

Group	Semester	Morning or afternoon session	Language	No. of enrolled students	
Gr. 401 (COMPUTER PRACTICALS) : 40 I2ADE	2S	Morning	Spanish	20	▪ Allowed INTERNATIONAL MOBILITY PROGRAMME ▪ Allowed VISITING STUDENT NO EEES ▪ Allowed VISITING STUDENT EEES ▪ Allowed DOUBLE DEGREE IN COMPUTER ENGINEERING AND BUSINESS ADMINISTRATION
Gr. 402 (COMPUTER PRACTICALS) : 402 I2ADE	2S	Morning	Spanish	20	

Timetables

THEORY CLASS

Group	Start date	End date	Day	Start time	End time	Lecture room
1	27/01/2025	23/05/2025	LUN	11:00	13:00	A3/0008
2	27/01/2025	23/05/2025	LUN	11:00	13:00	A3/0007
3	27/01/2025	23/05/2025	VIE	09:00	11:00	A3/0007
4	27/01/2025	23/05/2025	MAR	15:00	17:00	A3/0011
40	27/01/2025	23/05/2025	LUN	09:00	11:00	A2/E11

COMPUTER PRACTICALS

Group	Start date	End date	Day	Start time	End time	Lecture room
01	27/01/2025	23/05/2025	VIE	13:00	15:00	0039PS051
02	27/01/2025	23/05/2025	MAR	13:00	15:00	0039PS051
03	27/01/2025	23/05/2025	VIE	11:00	13:00	0039PS051
04	27/01/2025	23/05/2025	MAR	17:00	19:00	0039PS051
05	27/01/2025	23/05/2025	LUN	17:00	19:00	0039PS051
06	27/01/2025	23/05/2025	JUE	15:00	17:00	0039PS051
07	27/01/2025	23/05/2025	VIE	13:00	15:00	0039PB056
401	27/01/2025	23/05/2025	VIE	11:00	13:00	0016P1003
402	27/01/2025	23/05/2025	VIE	11:00	13:00	0016P1002